

EE 434

Lecture 37

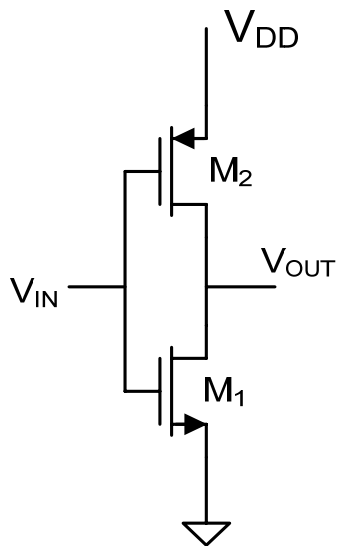
Propagation Delay in Logic Circuits

Power Dissipation

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy : Express delays in terms of those of reference inverter



Reference Inverter

$$C_{REF} = C_{IN} = 4C_{OX} W_{MIN} L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (V_{DD} - V_{Tn})} \stackrel{V_{Tn} = .2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN} (0.8V_{DD})}$$

$$t_{REF} = t_{HLREF} + t_{LHREF} = \frac{2 R_{PDREF} C_{REF}}{R_{PDREF}}$$

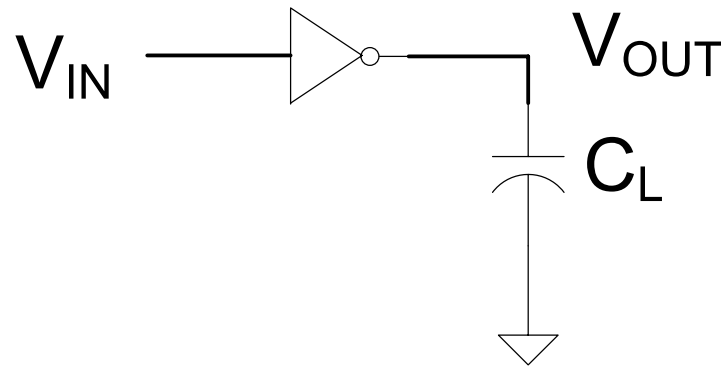
Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Capacitive Loading



Define the Fan In loading on the stage to be the total capacitive load on the stage normalized to C_{REF}

$$F_{IL} = \frac{C_L}{C_{REF}}$$

If inverter sized for equal rise/fall

$$t_{HL} = t_{LH} = R_{PD} C_L = R_{PD} C_{REF} F_{IL}$$

$$t_{PROP} = t_{LH} + t_{HL} = 2 R_{PD} C_{REF} F_{IL}$$

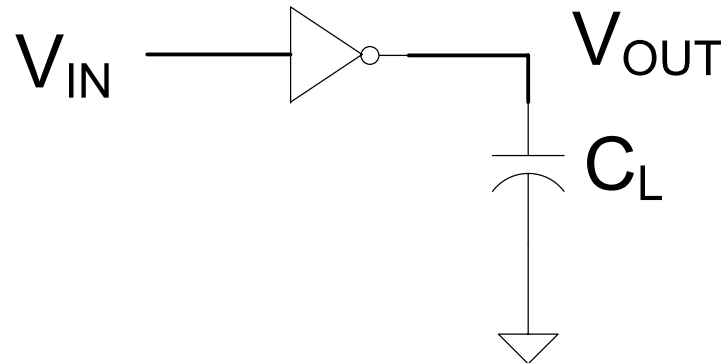
If inverter is the reference inverter

$$t_{PROP} = t_{REF} F_{IL}$$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive



Define the Overdrive Factor of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

$$R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \quad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}$$

If inverter sized for equal rise/fall, $OD_{HL} = OD_{LH} = OD$

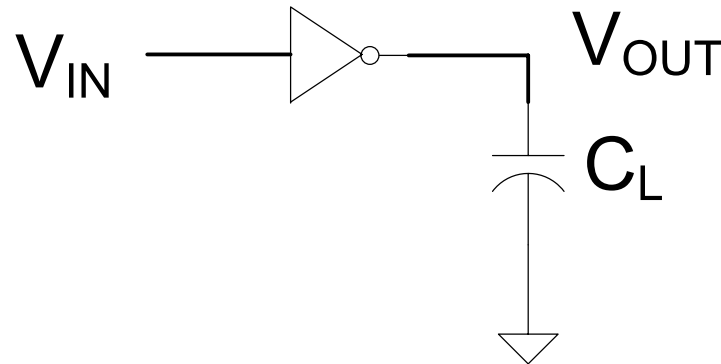
$$t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_L = \frac{R_{PDREF}}{OD} C_{REF} \frac{F_{IL}}{OD}$$

$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

OD may be larger or smaller than 1

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive



$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

If inverter is not equal rise/fall

$$t_{HL} = \frac{R_{PDREF}}{OD_{HL}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{HL}}$$

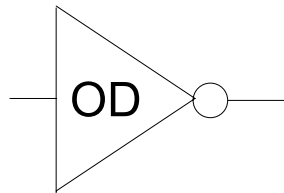
$$t_{LH} = \frac{R_{PUREF}}{OD_{LH}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{LH}}$$

$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

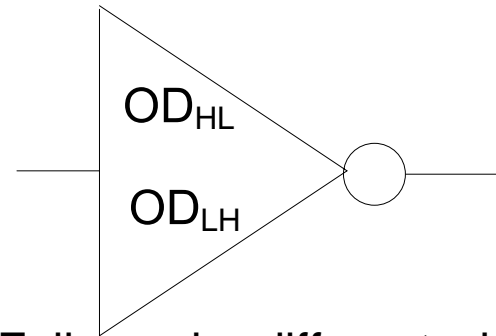
Handwritten red notes:
 $2 R_{PDREF} C_{REF} = t_{REF}$
 $R_{PUREF} = \frac{1}{2} \frac{t_{REF}}{C_{REF}}$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

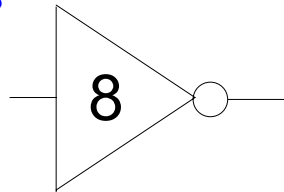


Equal Rise/Fall with overdrive OD

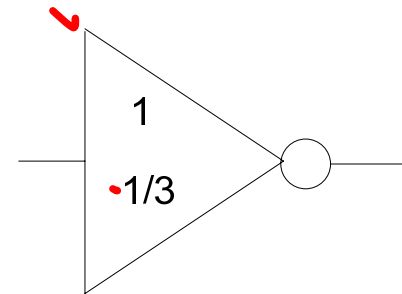


Rise/Fall may be different with overdrive OD_{HL} and OD_{LH}

Examples



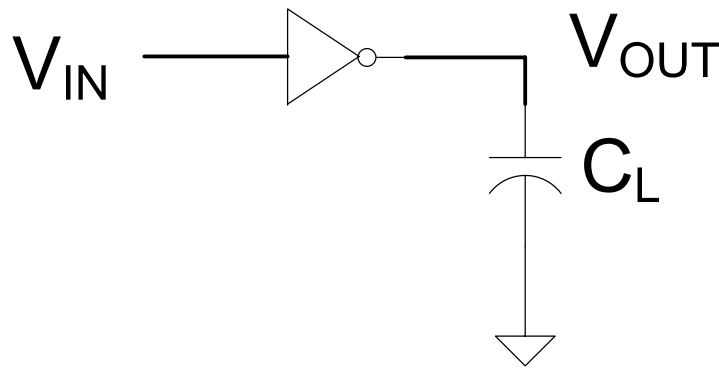
Equal Rise/Fall with overdrive of 8



If $W_n = W_{MIN}$, minimum sized inverter

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example:



$$t_{\text{PROP}} = t_{\text{LH}} + t_{\text{HL}} = t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}}$$

If inverter is not equal rise/fall

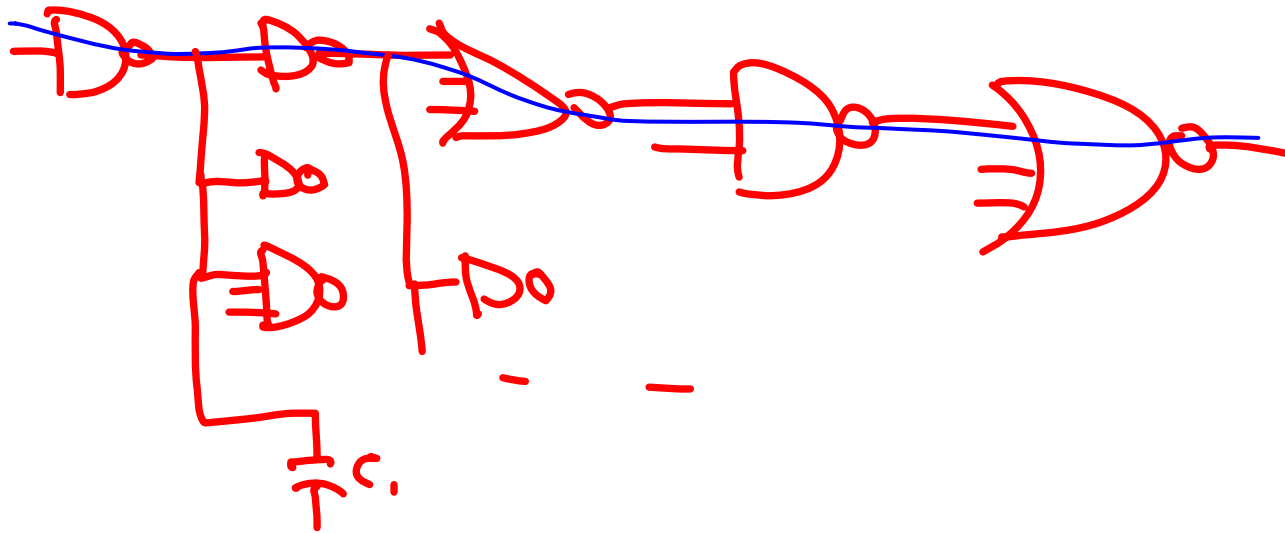
$$t_{\text{HL}} = \frac{R_{\text{PDREF}}}{\text{OD}_{\text{HL}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{HL}}}$$

$$t_{\text{LH}} = \frac{R_{\text{PUREF}}}{\text{OD}_{\text{LH}}} C_L = \frac{1}{2} t_{\text{REF}} \frac{F_{\text{IL}}}{\text{OD}_{\text{LH}}}$$

$$t_{\text{PROP}} = t_{\text{HL}} + t_{\text{LH}} = \frac{1}{2} t_{\text{REF}} F_{\text{IL}} \left(\frac{1}{\text{OD}_{\text{HL}}} + \frac{1}{\text{OD}_{\text{LH}}} \right)$$



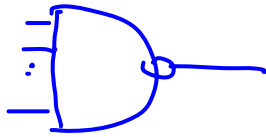
Propagation Delay in Multiple-Levels of Logic with Stage Loading



for m levels of logic

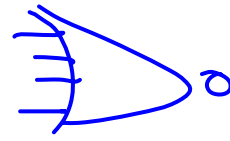
$$t_{\text{PROP}} = \sum_{i=1}^m t_{\text{PROP}_i} = t_{\text{REF}} \sum_{i=1}^m \frac{FI_{i+1}}{OO_i}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



$$C_{IN} = \frac{3+k}{4} C_{REF}$$

$$F_{IL} = \frac{3+k}{4}$$



$$C_{IN} = \frac{3k+1}{4} C_{REF}$$

$$F_{IL} = \frac{3k+1}{4}$$

NAND gates cause considerably less loading than NOR gates for large number of inputs with equal rise & fall times



$$F_{IL} = m \left(\frac{3+k}{4} \right)$$



$$F_{IL} = m \left(\frac{3k+1}{4} \right)$$

$$C_{REF} = 4C_0 + W_{min} / L_{min}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

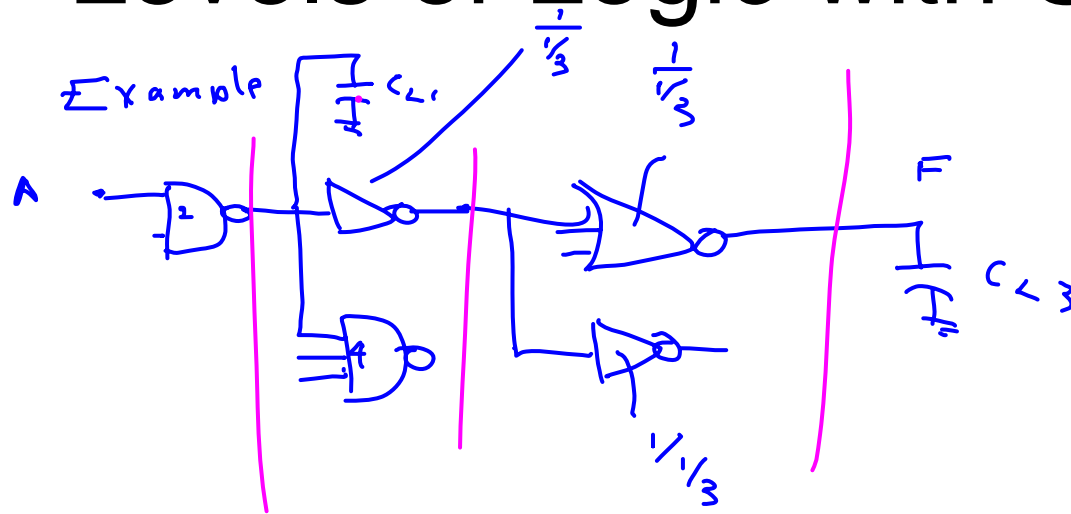
Propagation delay with non-equal rise and fall times

$$\text{Recall } t_{PROP} = t_{REF} \sum_{i=1}^m \frac{F_{ILi+1}}{OD_i} = \underbrace{t_{REF}}_2 \sum_{i=1}^m \frac{F_{SLi+1}}{OD} + \underbrace{t_{REF}}_2 \sum_{i=1}^m \frac{F_{ILi+1}}{OD}$$

$$t_k = \frac{t_{REF}}{2} \frac{F_{ILk+1}}{OD_{HL}} + \frac{t_{REF}}{2} \frac{F_{ILk+1}}{OD_{LH}}$$

$$t_{PROP} = \sum_{k=1}^m t_k = \frac{t_{REF}}{2} \sum_{k=1}^m F_{ILk+1} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



Recall:

$$C_{in, \text{NOR}} = \frac{3(k+1)}{4} C_{REF}$$

$$C_{in, \text{NAND}} = \frac{k+3}{4} C_{REF}$$

$$C_{in, \text{min}} = \frac{C_{REF}}{2}$$

$$t_{prop} = t_1 + t_2 + t_3$$

$$t_1 = t_{REF} \left(\frac{C_{L1}}{C_{REF}} + \frac{1}{2} + \left(\frac{6}{4} \right) (4) \right)$$

$$t_2 = \frac{t_{REF}}{2} \left[\frac{1}{2} + \frac{1}{2} \right] \left[\frac{1}{1} + \frac{1}{3} \right]$$

$$t_3 = \frac{t_{REF}}{2} \left[\frac{C_{L3}}{C_{REF}} \right] \left[\frac{1}{1} + \frac{1}{3} \right]$$

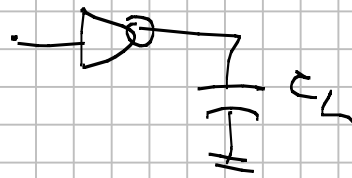
Propagation Delay in Multiple-Levels of Logic with Stage Loading

How can large loads be rapidly driven.

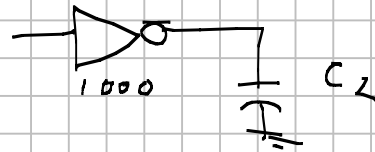
Recall:

$f_{HL} = 10000$

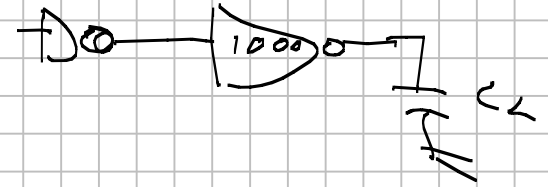
~~NA~~



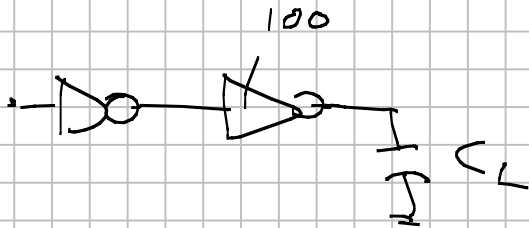
$t_{PROP} = (t_{REF}) 10000$



$t_{PROP} = t_{REF}$



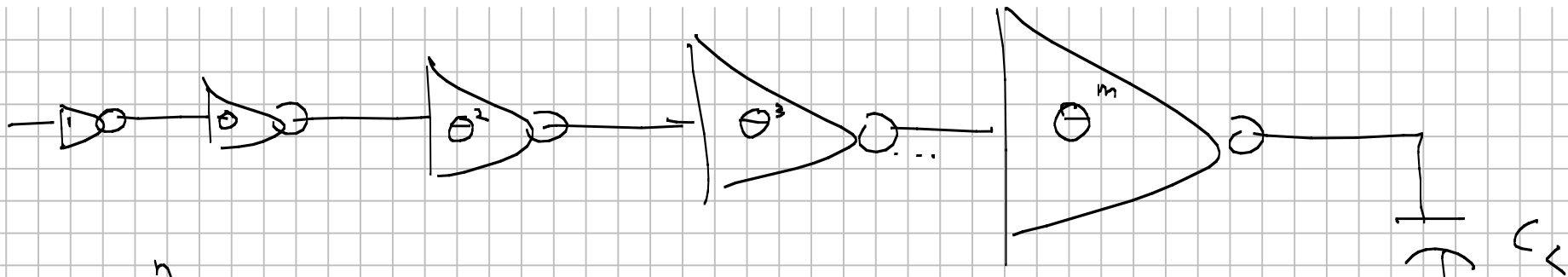
$t_{PROP} = (001) t_{REF}$



$t_{PROP} = 200 t_{REF}$

Dramatic Improvement

- multiple levels of logic do not necessarily increase overall delay



$$C_L = \Theta^n C_{REF}$$



$$t_{PROP} = \Theta^n t_{REF}$$

$$\begin{aligned}
 t_{CASCADE} &= t_{REF} \left(\frac{\Theta}{1} + \frac{\Theta^2}{\Theta} + \frac{\Theta^3}{\Theta^2} + \dots \right) \\
 &= t_{REF} (\Theta + \Theta + \Theta \dots + \Theta) \\
 &= t_{REF} n \Theta
 \end{aligned}$$

$$r = \frac{t_{CASCADE}}{t_{DIRECT}} = \frac{n \Theta t_{REF}}{\Theta^n t_{REF}} = n \Theta \quad \Rightarrow \quad 1 - n$$

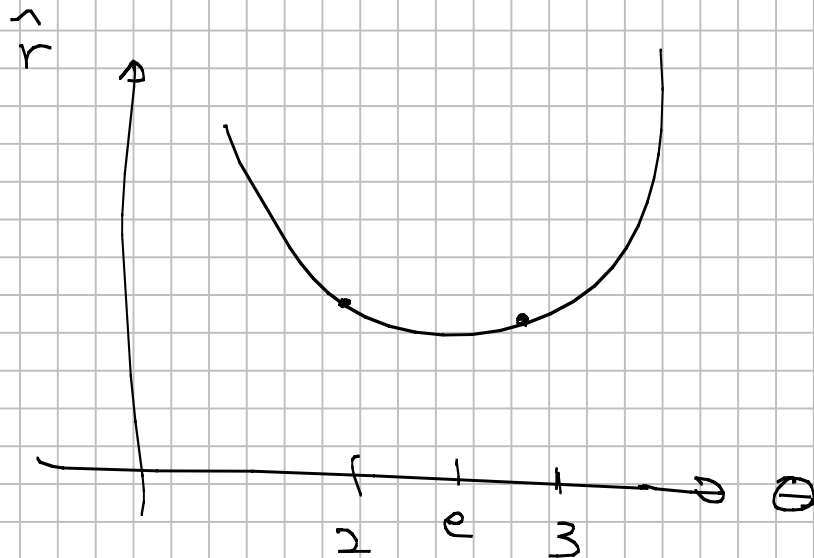
$$\begin{aligned}
 n, \Theta \quad \Theta^n C_{REF} &= C_L \\
 n \ln \Theta &= \ln \left(\frac{C_L}{C_{REF}} \right)
 \end{aligned}$$

$$r = \frac{\ln \frac{C_L}{C_{REF}}}{\ln \Theta} = \frac{\ln \frac{C_L}{C_{REF}}}{\ln \frac{C_L}{C_{REF}}} \left(\frac{\Theta}{1} \right)$$

$$\hat{r} = \frac{\theta}{\ln \theta}$$

$$\frac{\partial \hat{r}}{\partial \theta} = \frac{\ln \theta - \theta \left(\frac{1}{\theta}\right)}{(\ln \theta)^2} = 0 \Rightarrow \ln \theta = 1$$

$$\theta = e$$



Practically: use
OD of 2 to 3